

FIG. 1

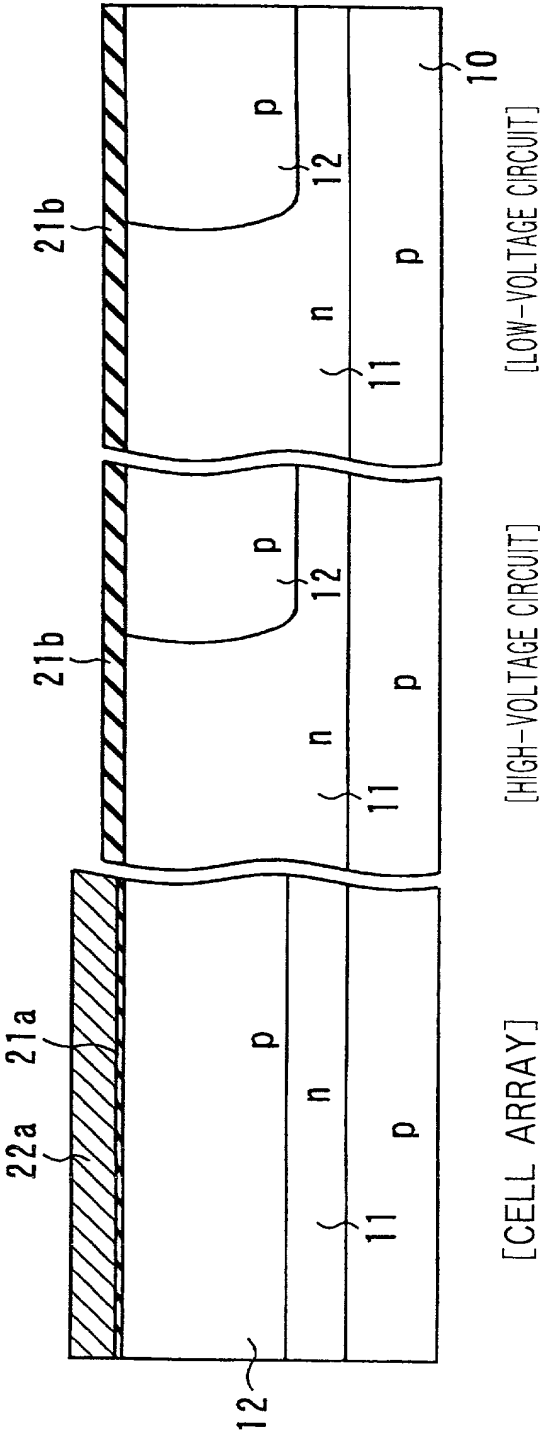


FIG. 2

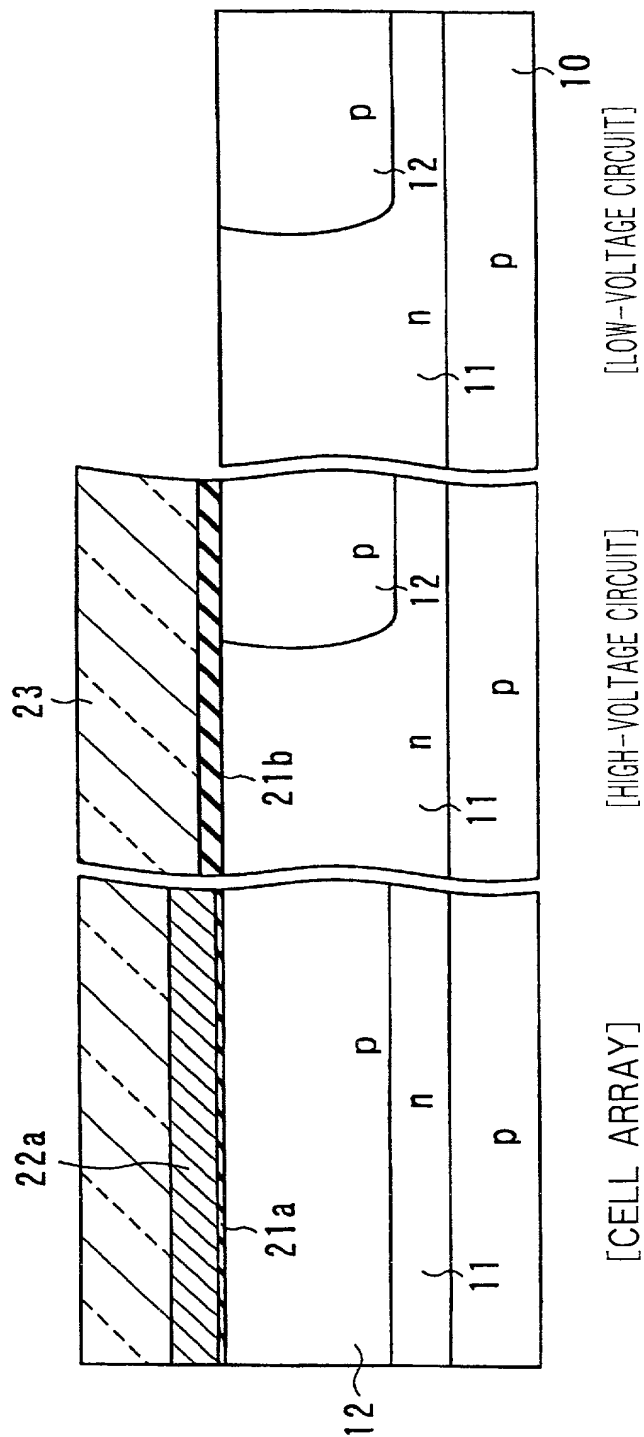


FIG. 3

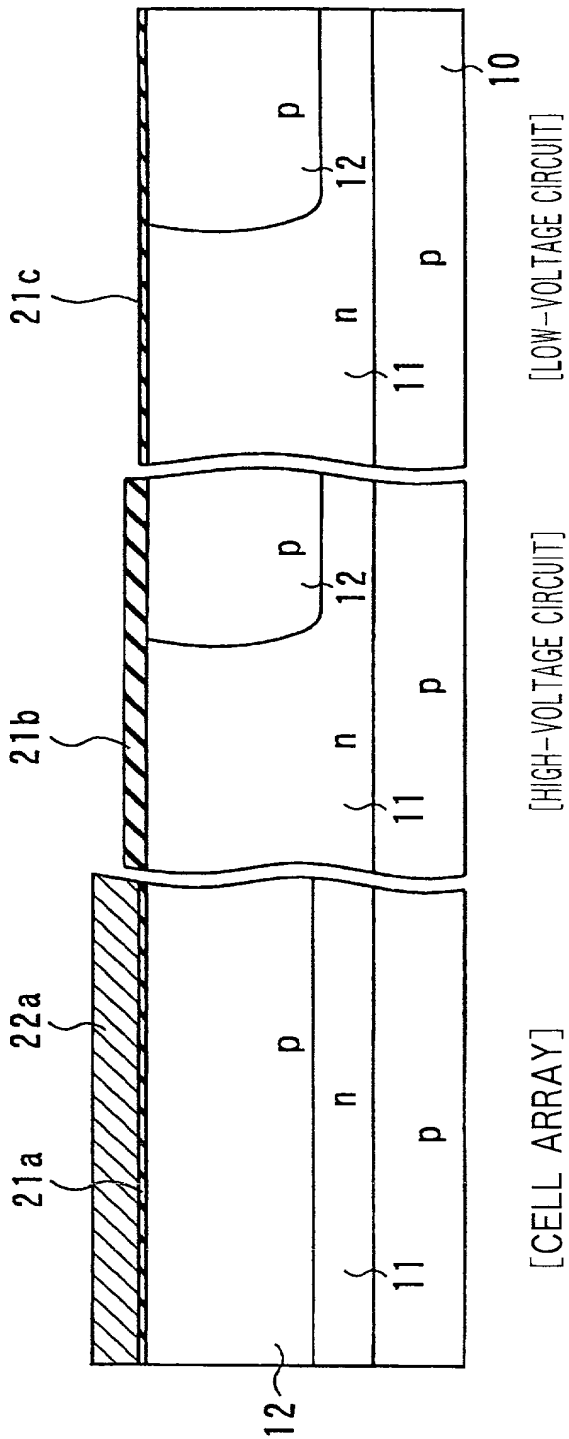


FIG. 4

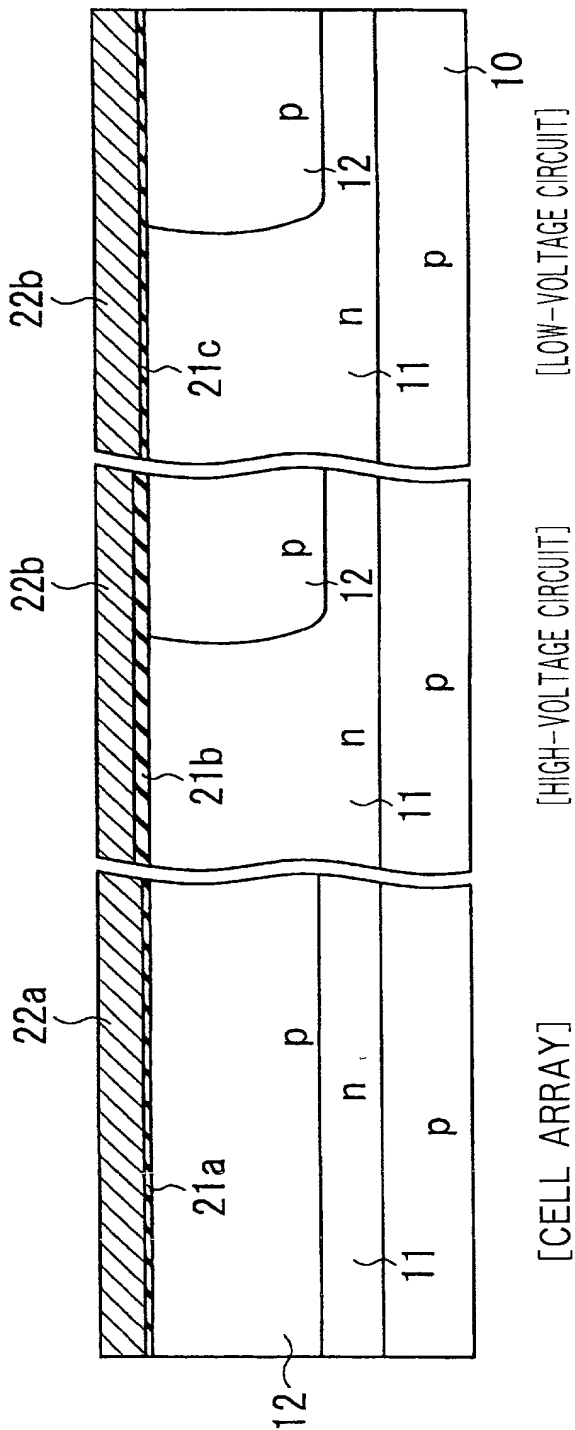


FIG. 5

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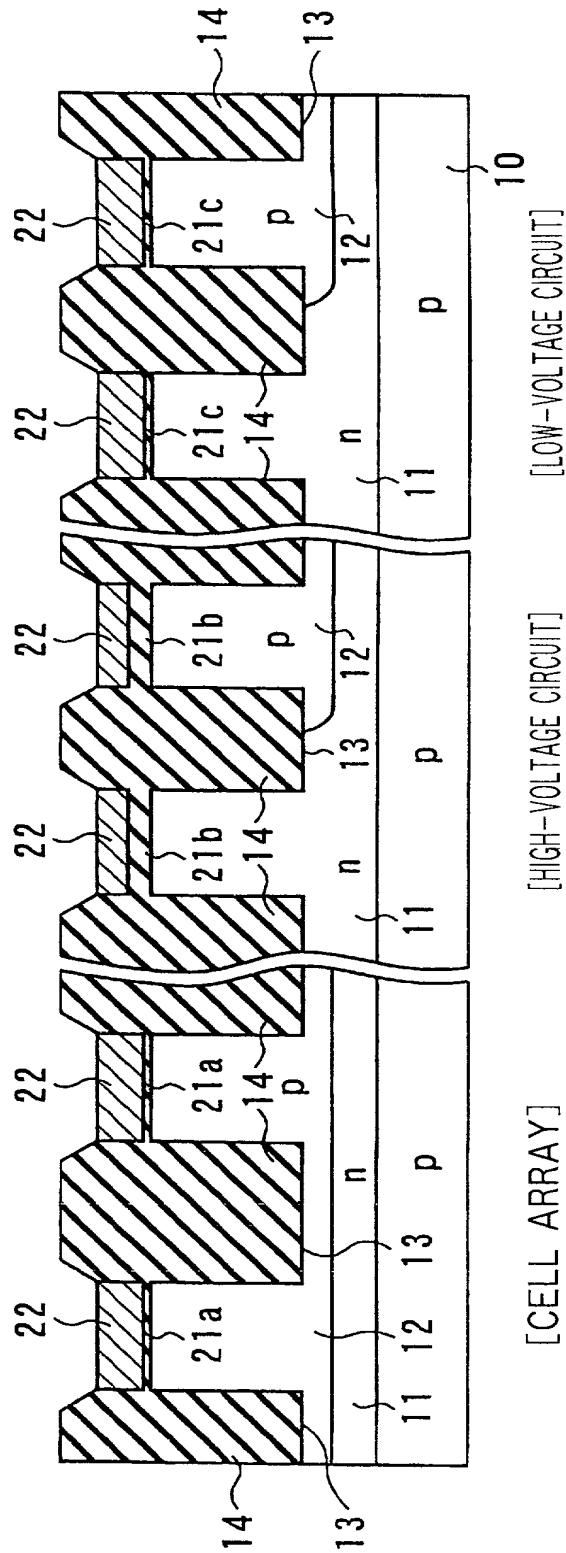


FIG. 6

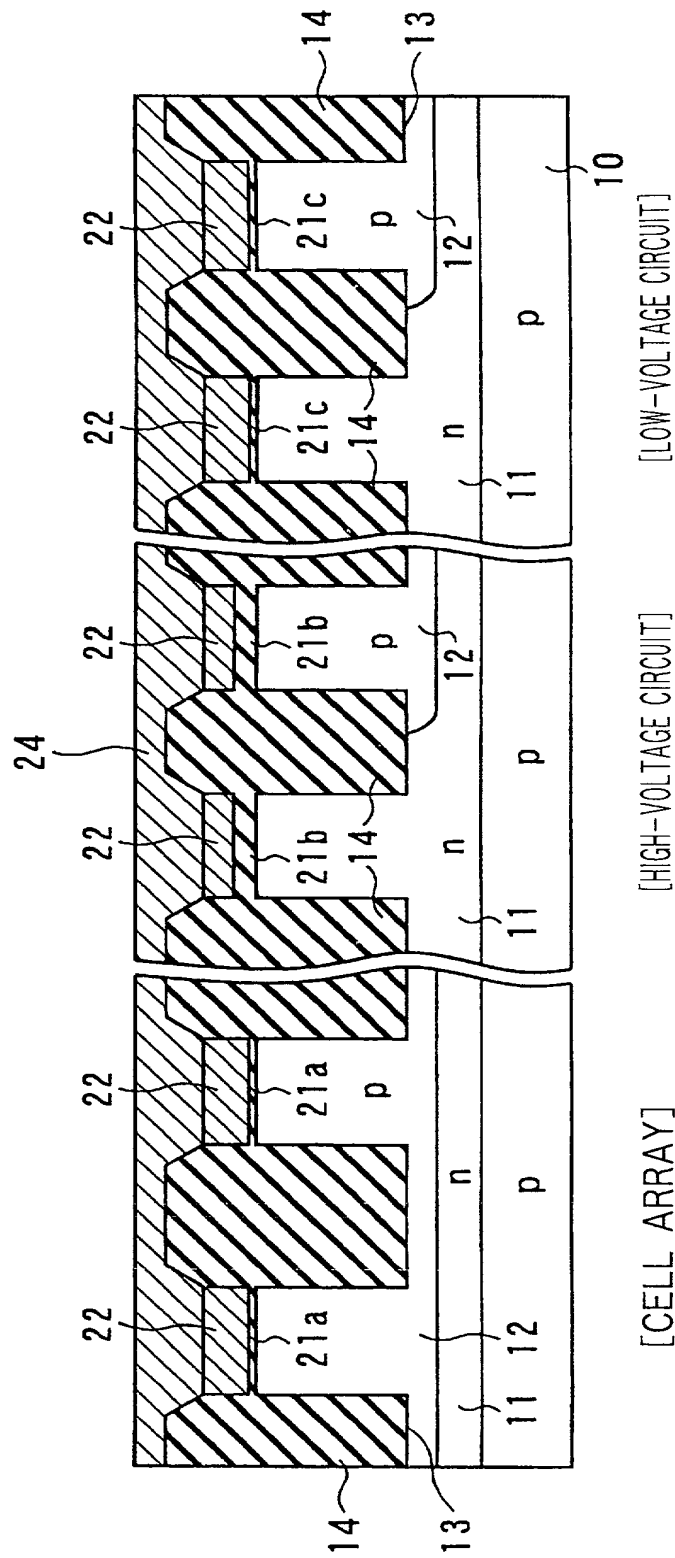


FIG. 7

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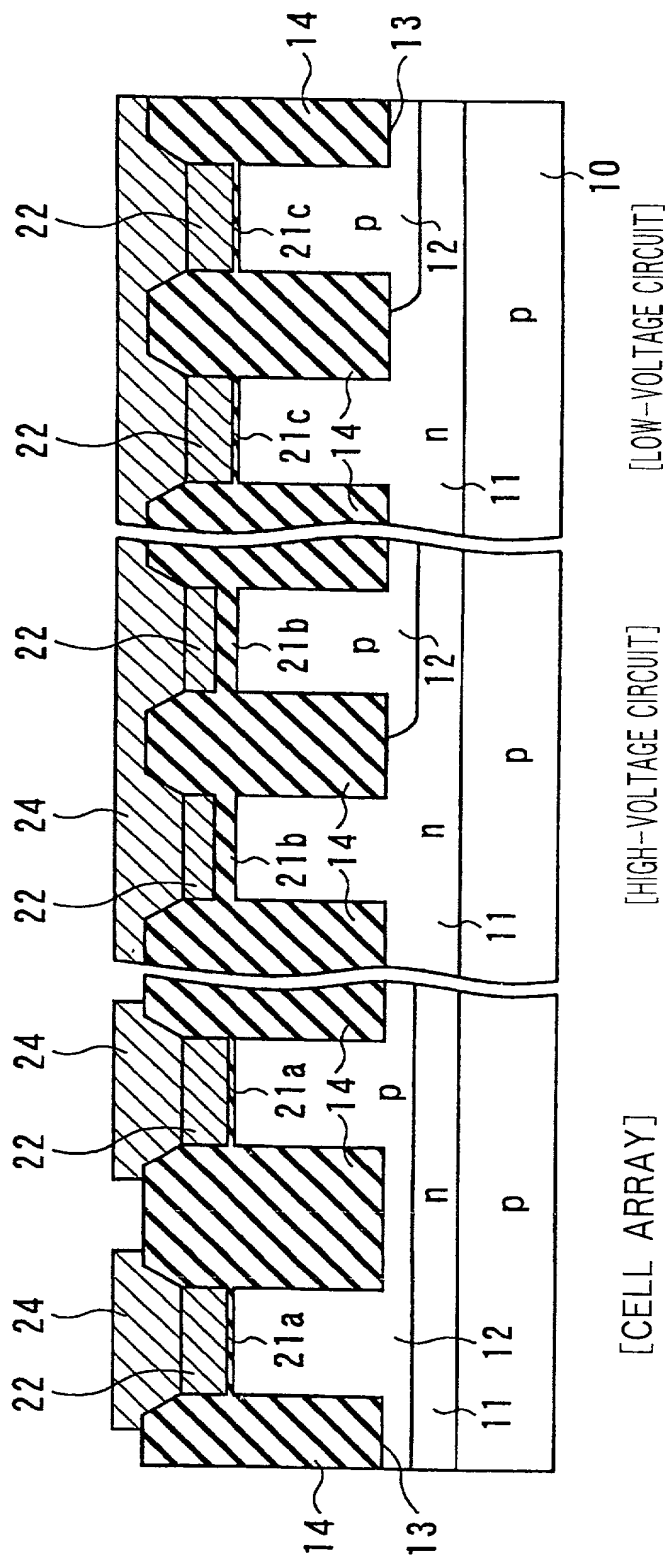


FIG. 9

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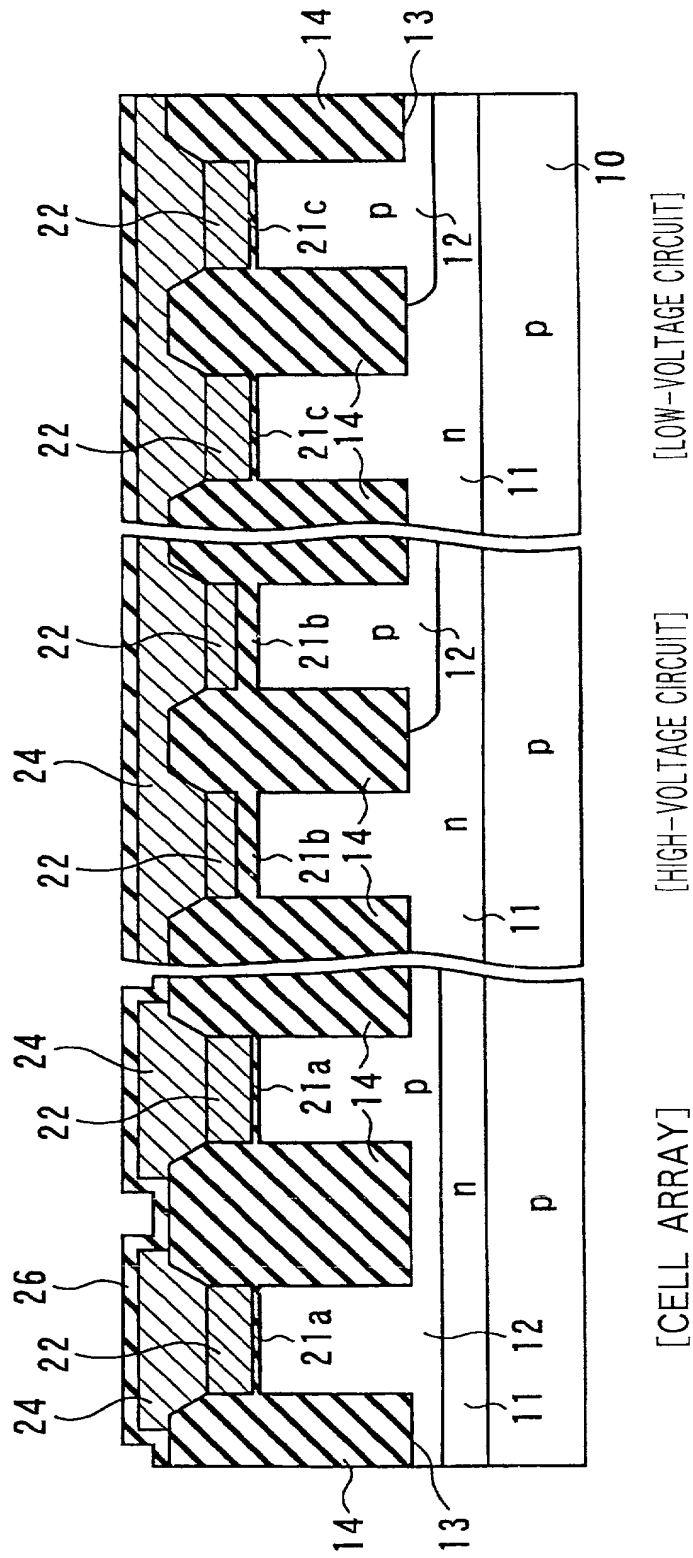


FIG. 10

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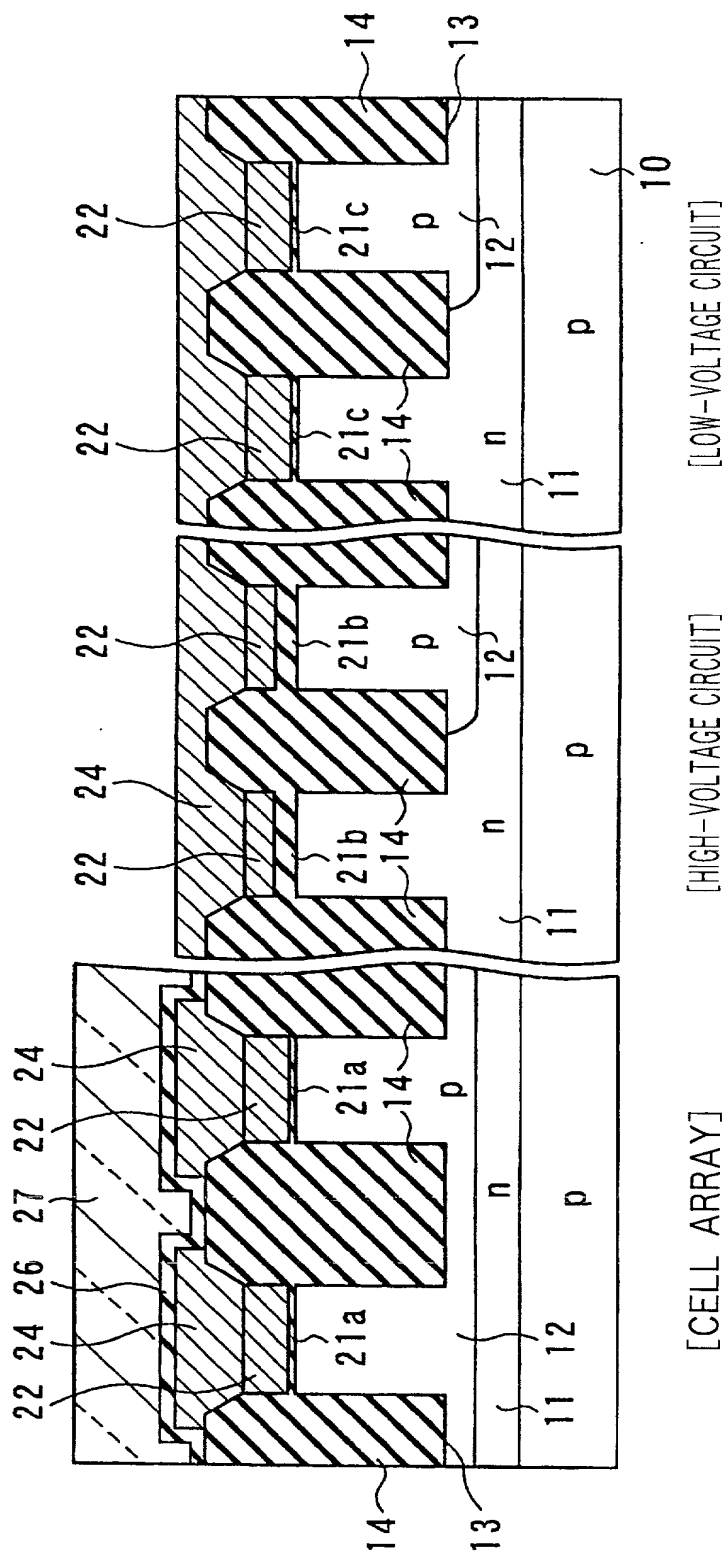


FIG. 11

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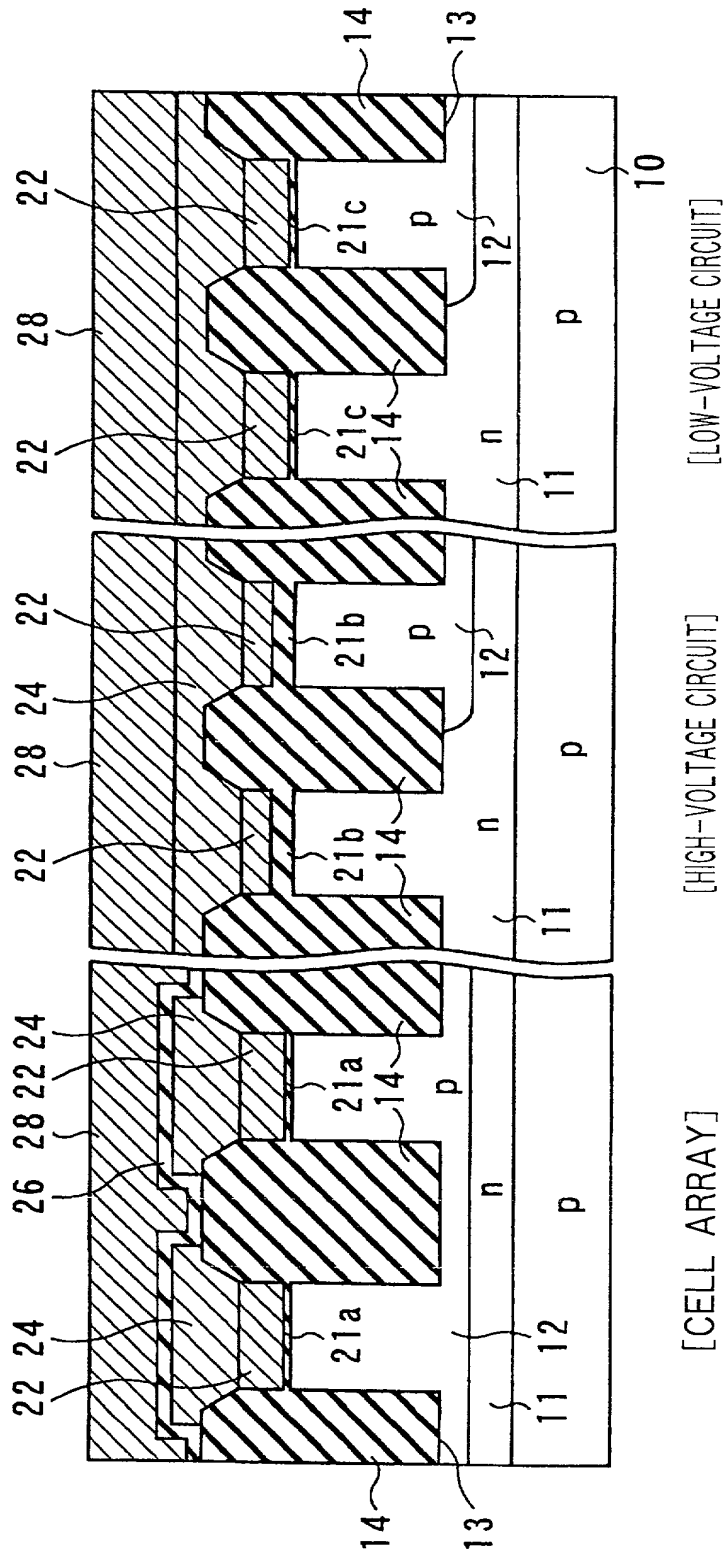


FIG. 12

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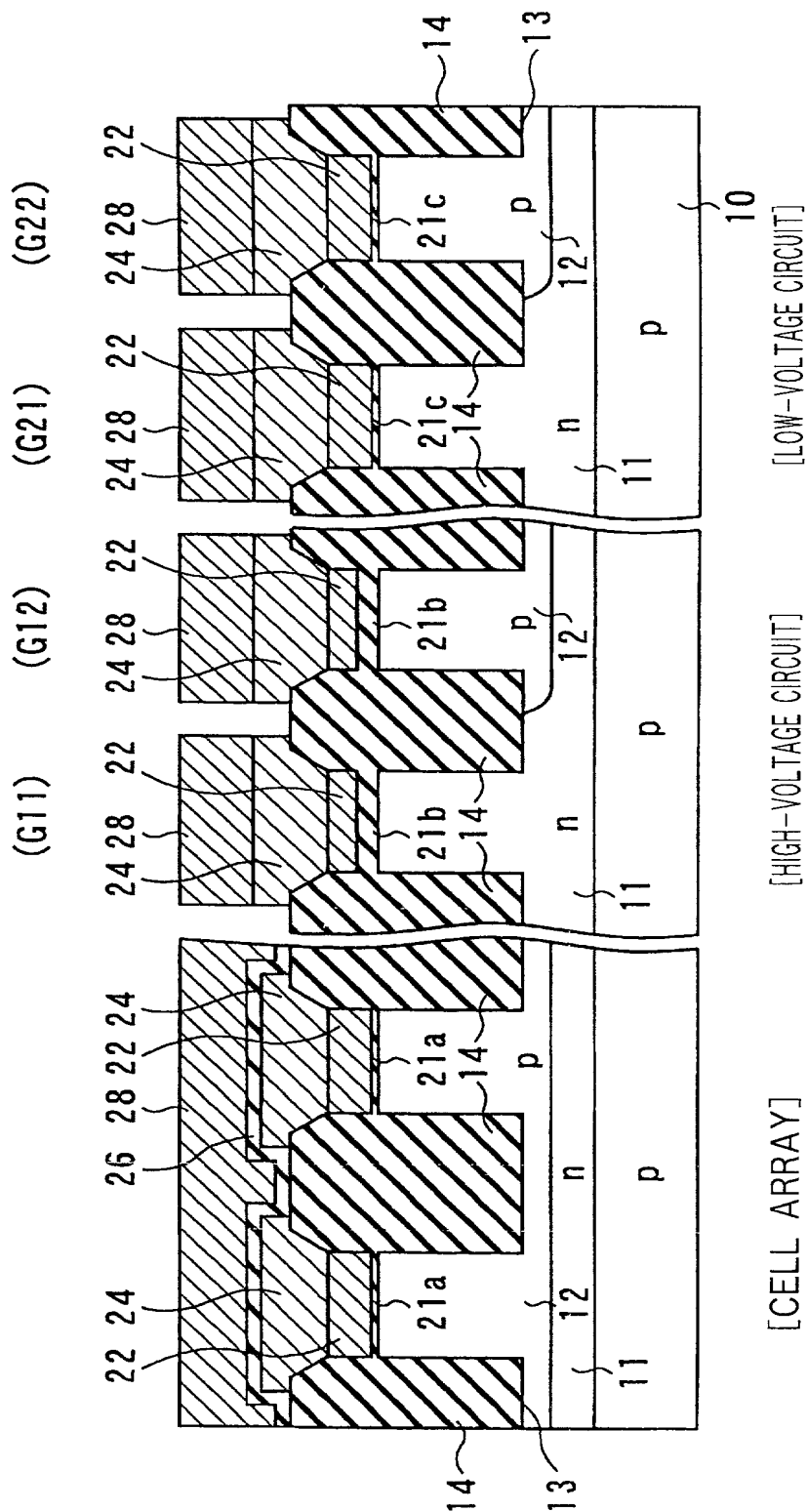


FIG. 13

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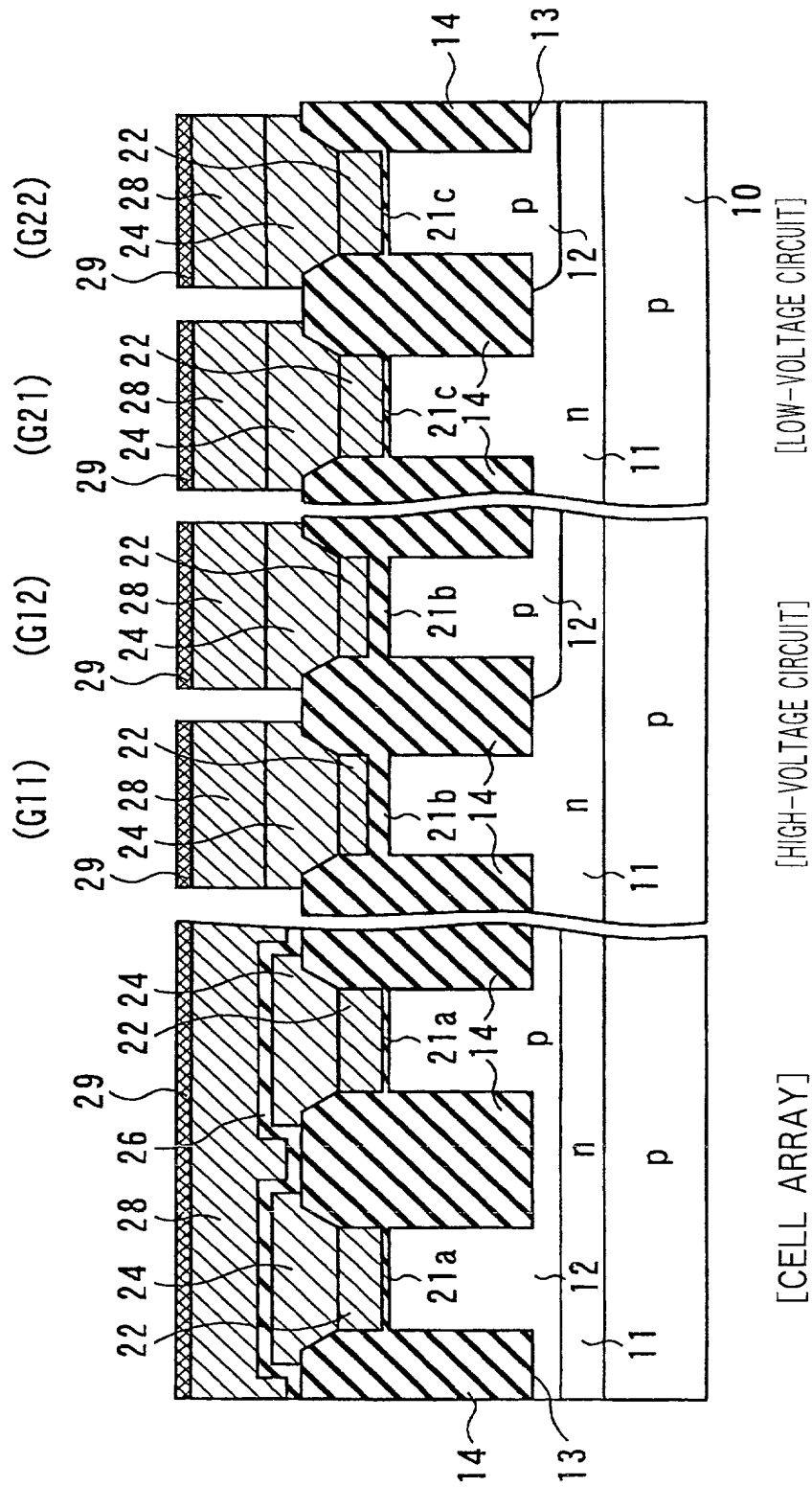


FIG. 14

FIG. 14A

FIG. 14B

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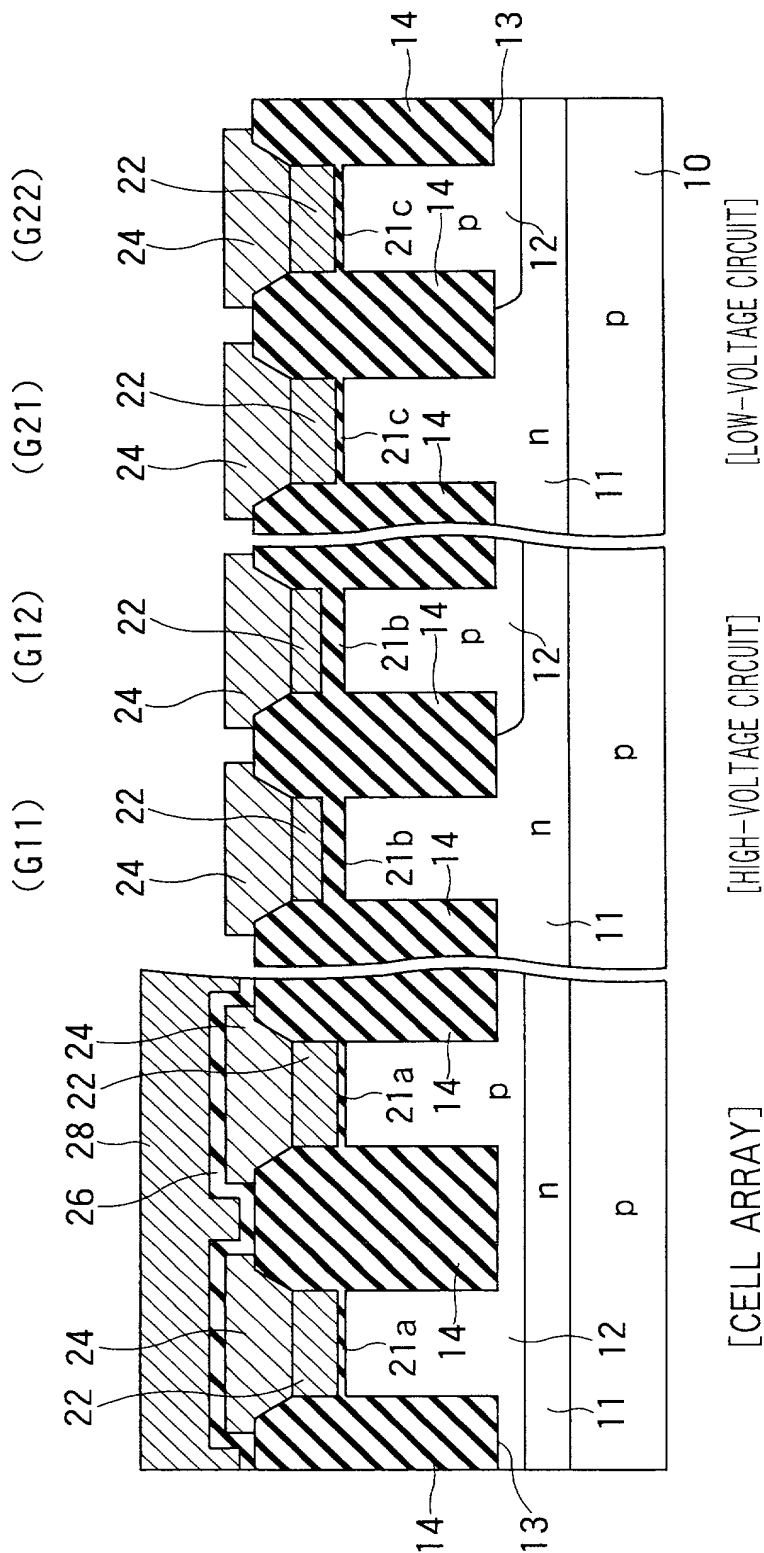


FIG. 14C

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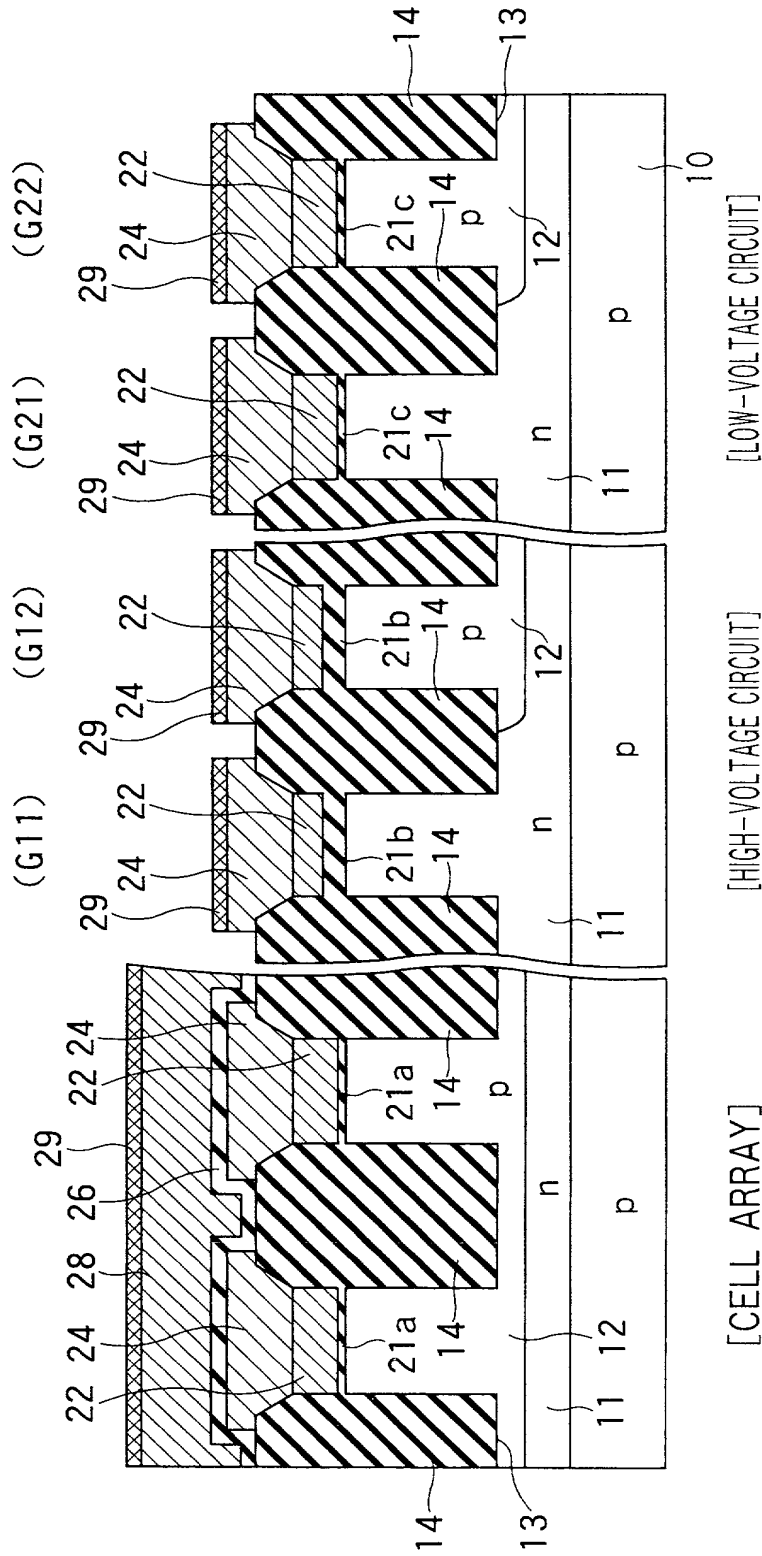
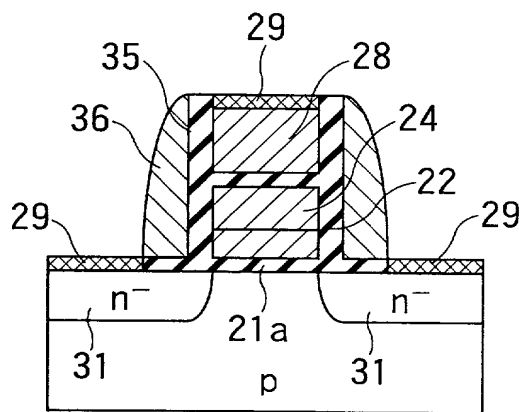
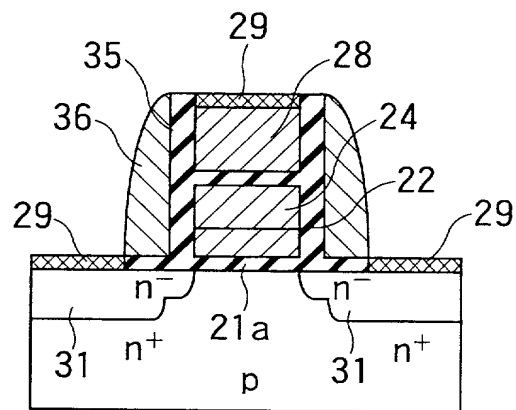


FIG. 14D

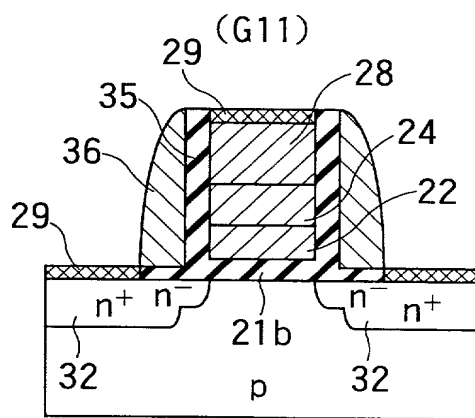
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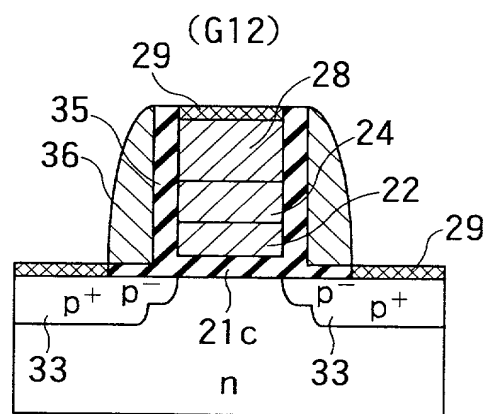
[MEMORY CELL]



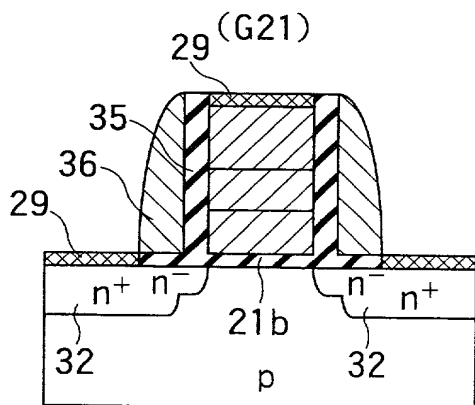
[MEMORY CELL]



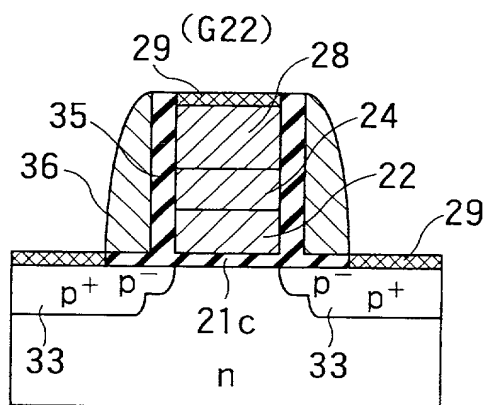
[HIGH-VOLTAGE NMOS]



[HIGH-VOLTAGE PMOS]



[LOW-VOLTAGE NMOS]



[LOW-VOLTAGE PMOS]

FIG. 15

FIG. 15

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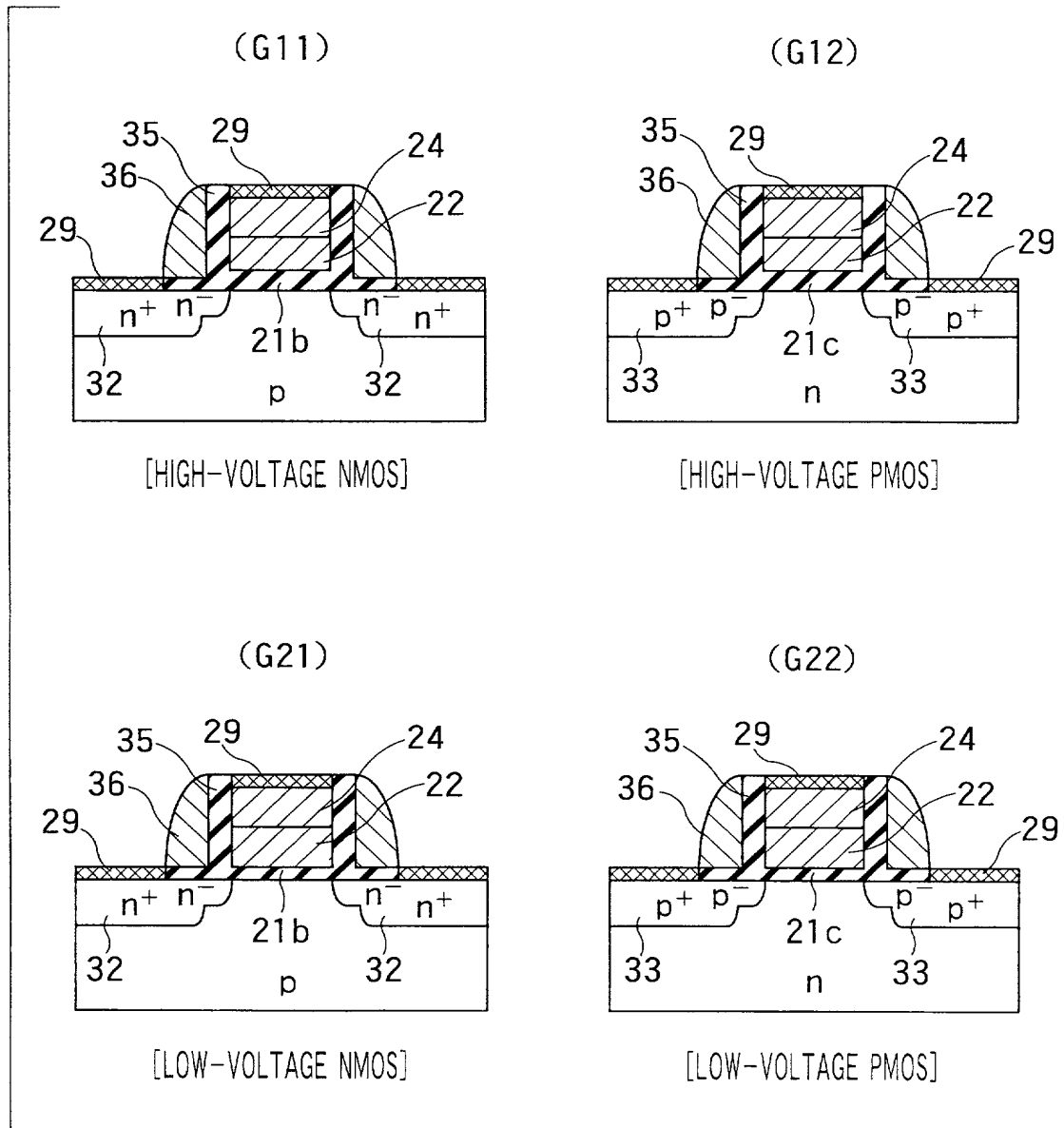


FIG. 15A

FIG. 16

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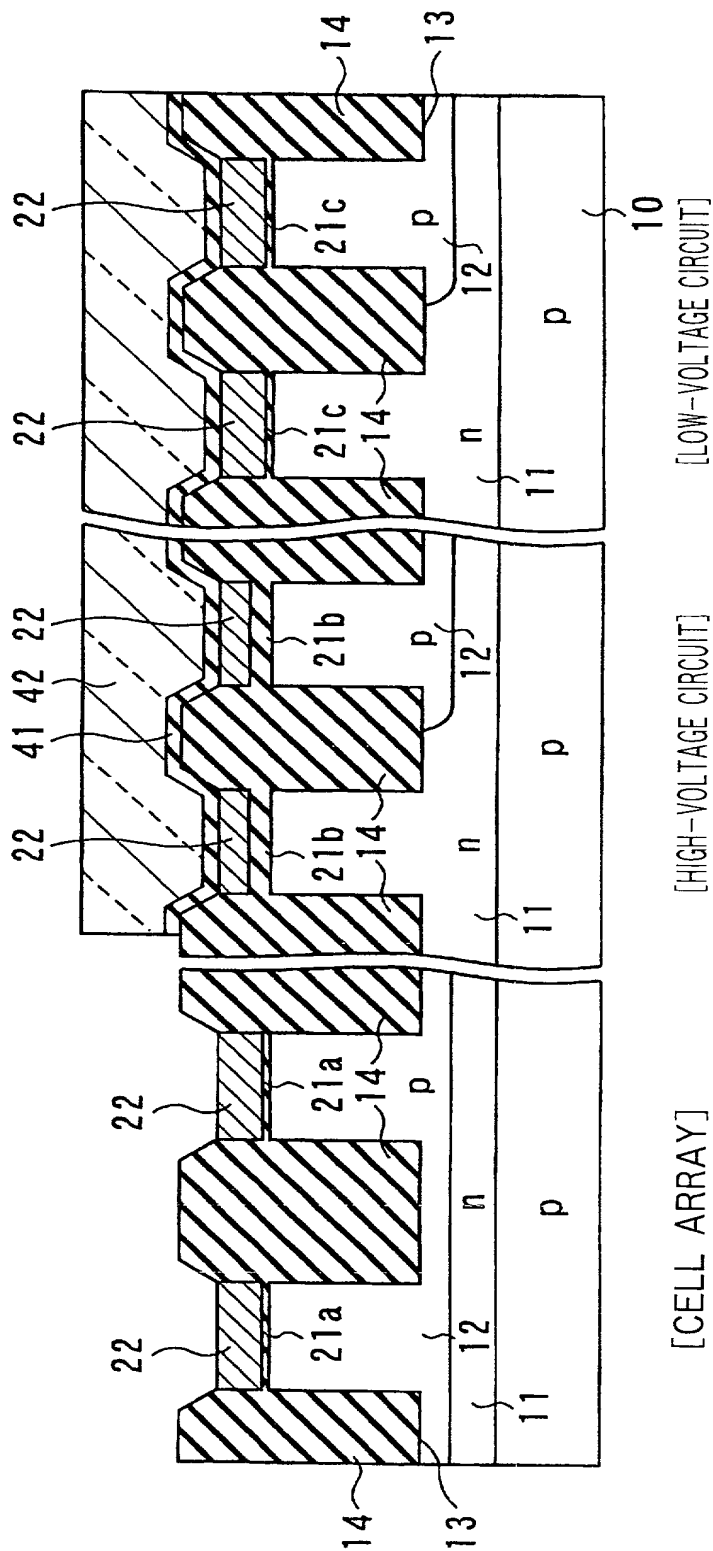


FIG. 17

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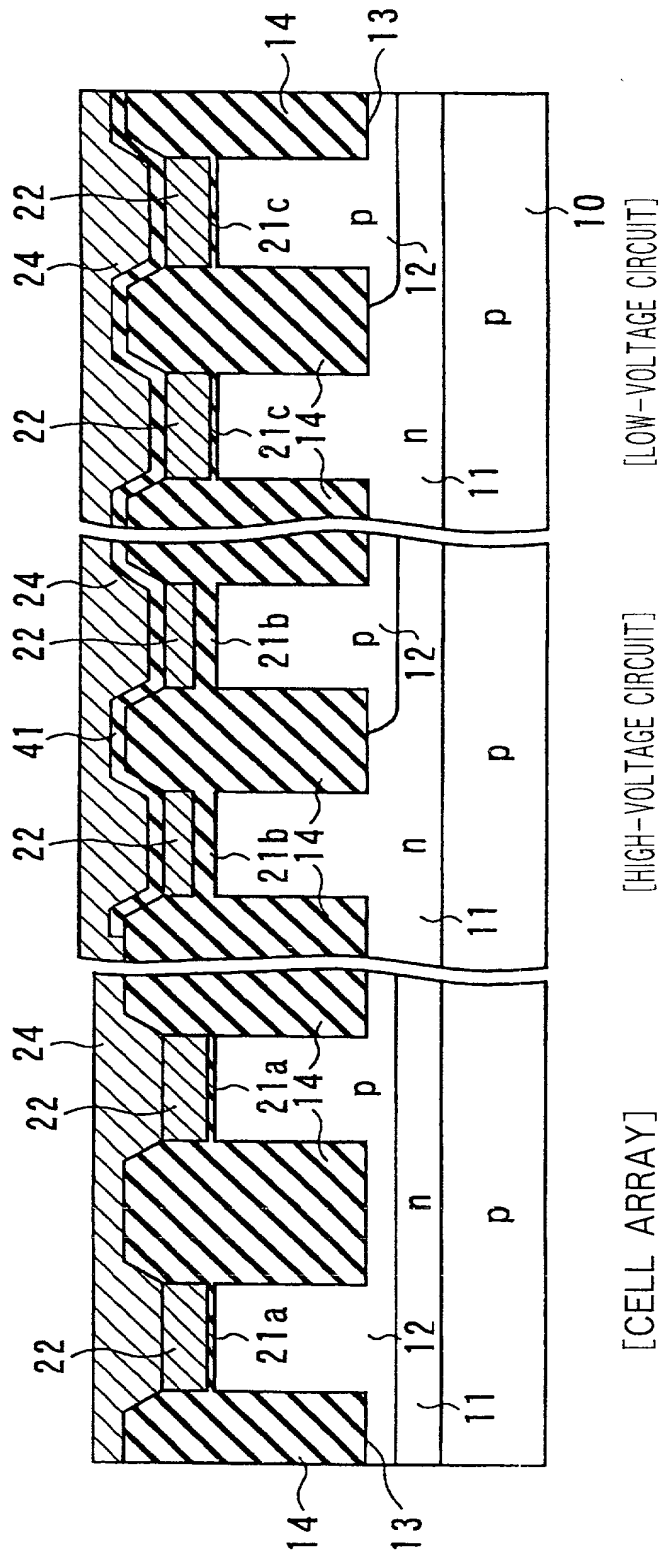


FIG. 18

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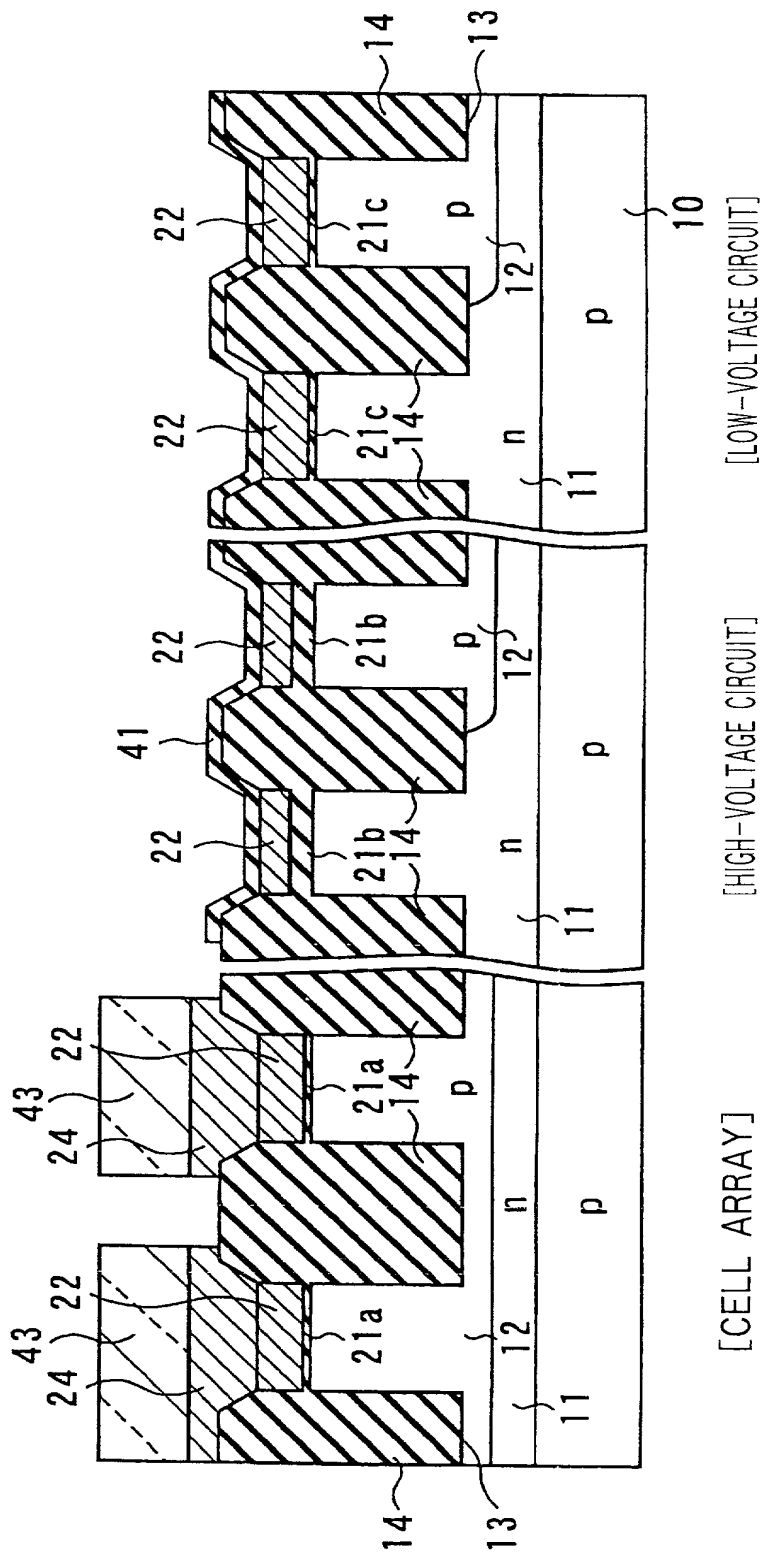


FIG. 19

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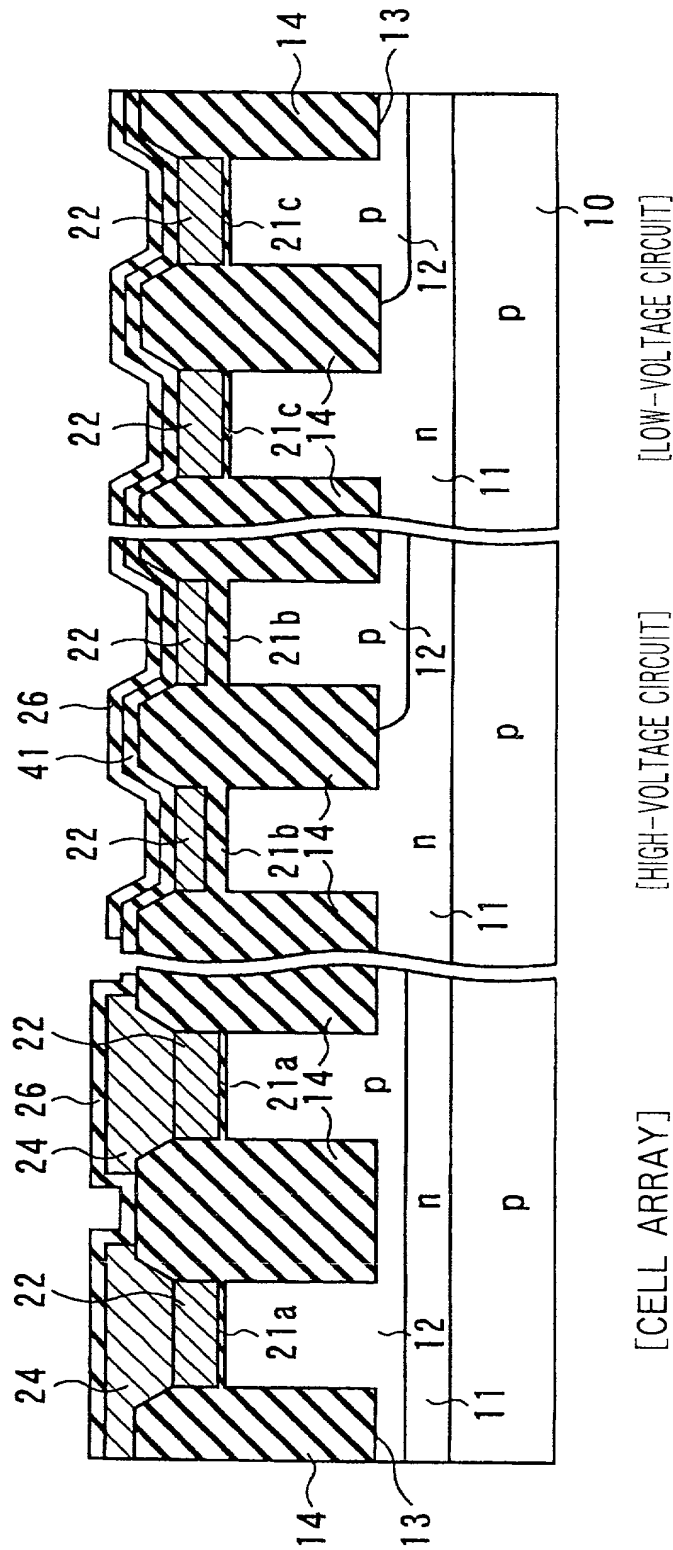


FIG. 20

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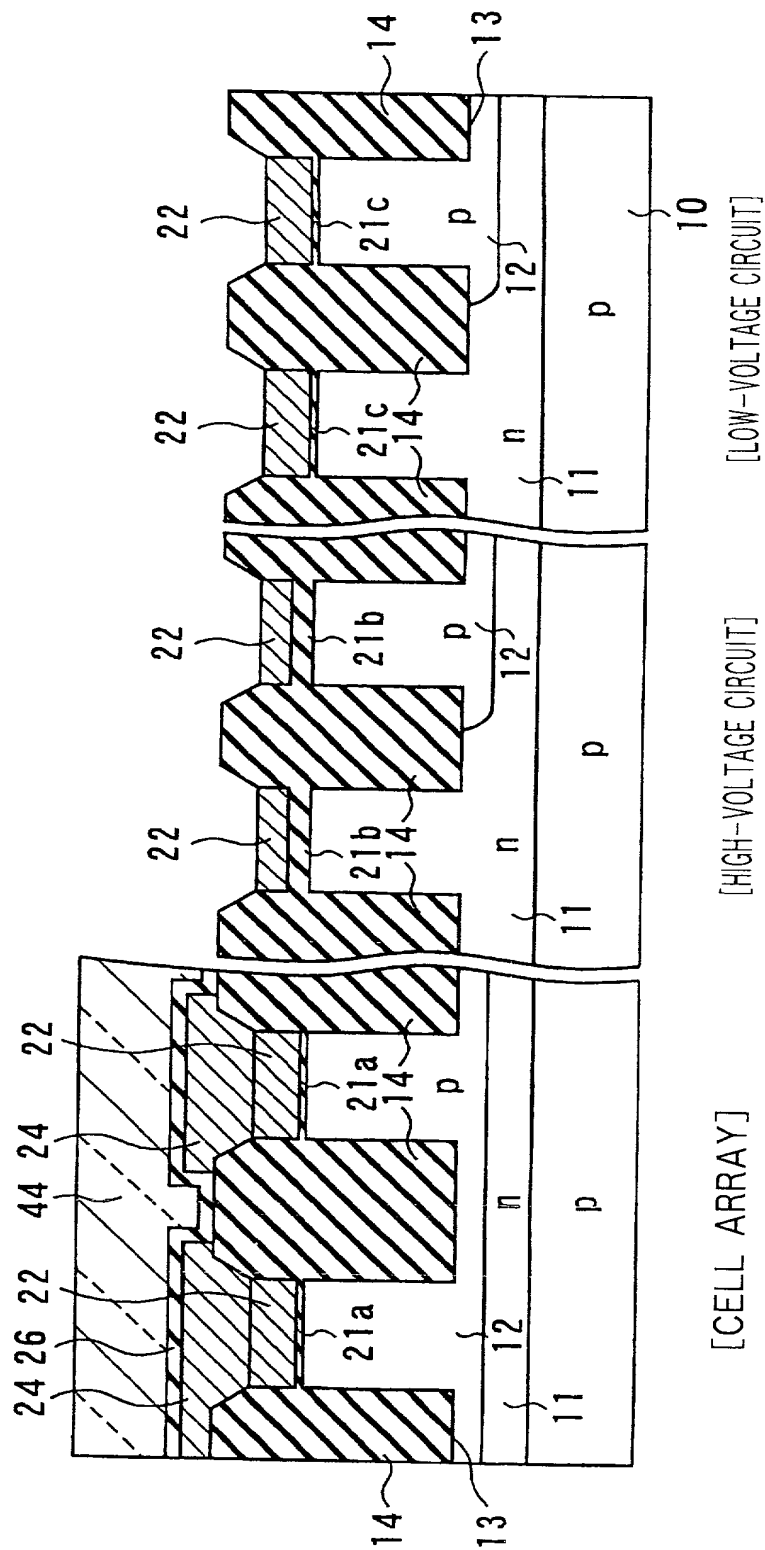


FIG. 21

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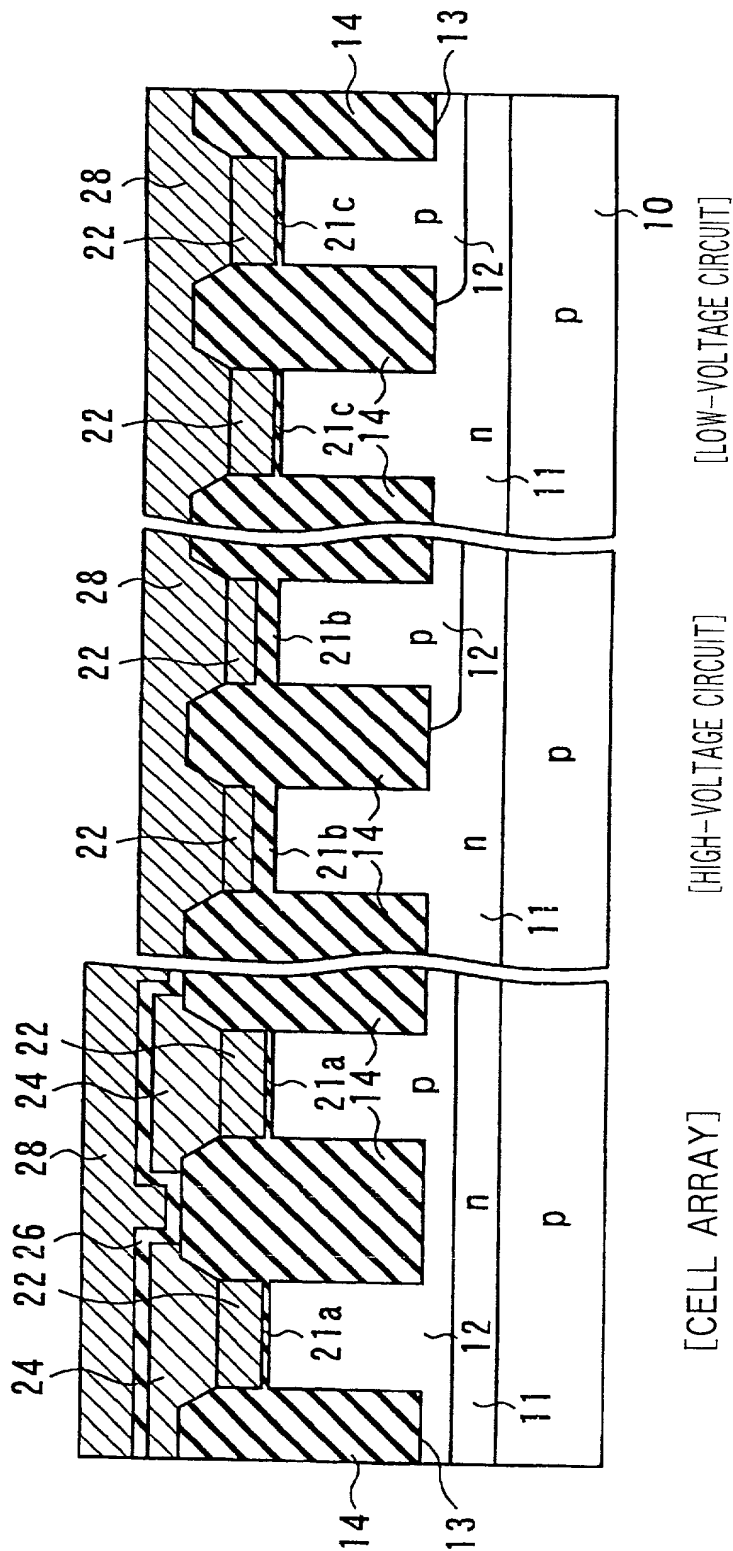


FIG. 22

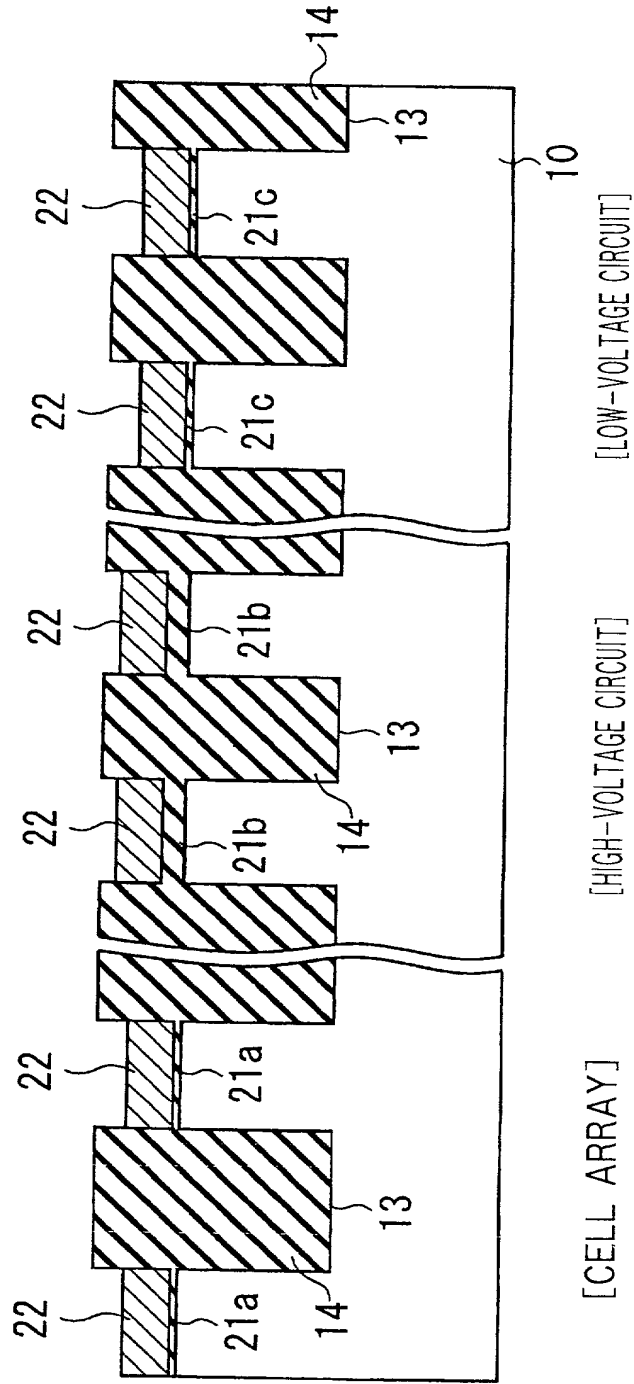


FIG. 23

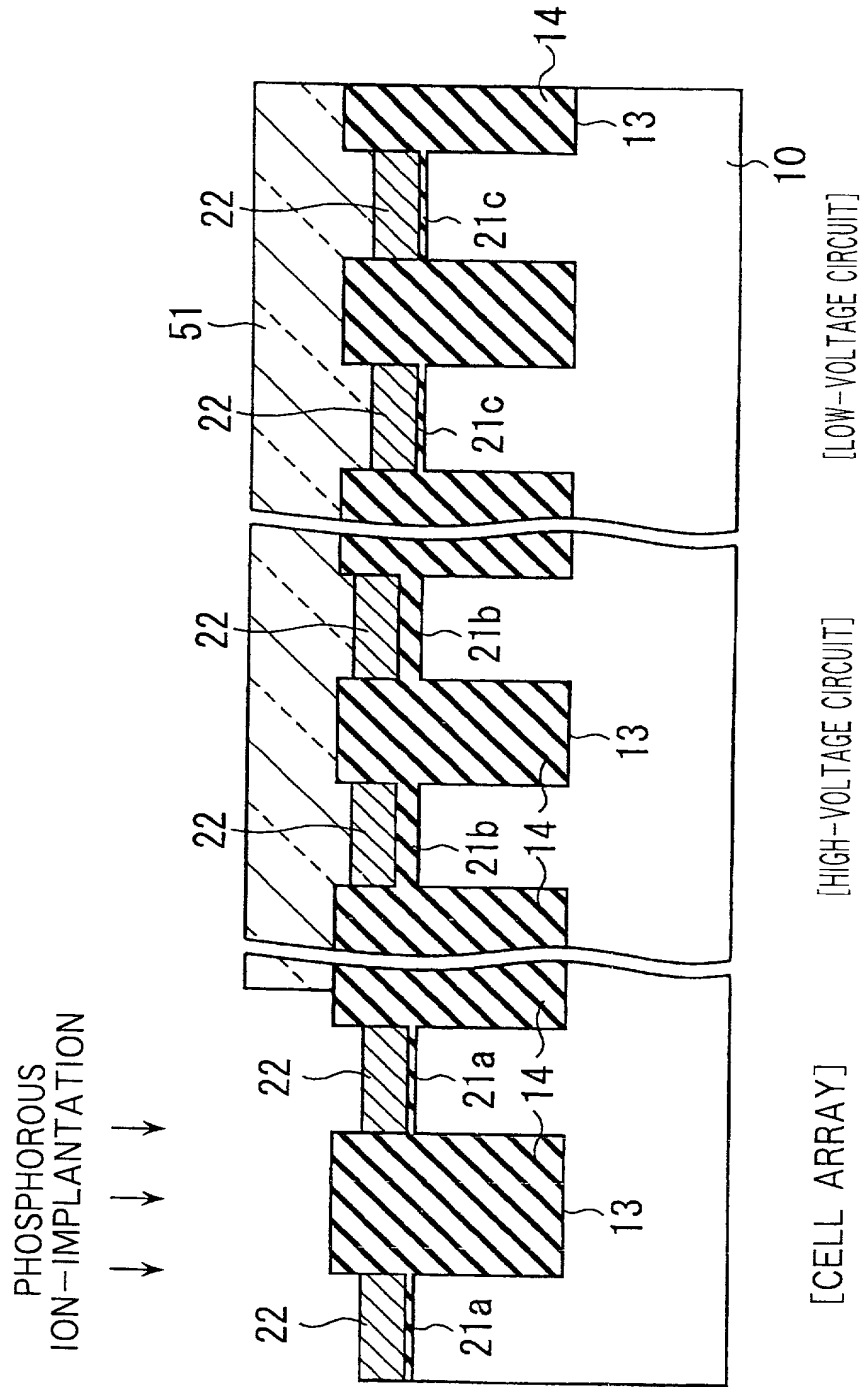


FIG. 24

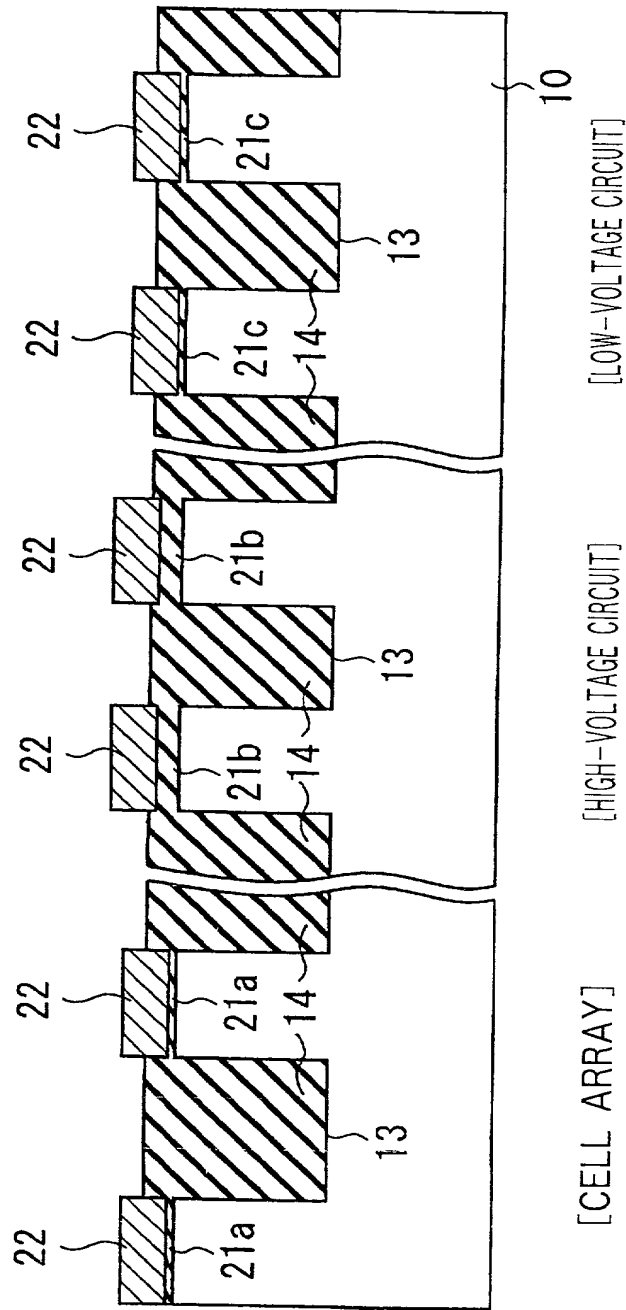


FIG. 25

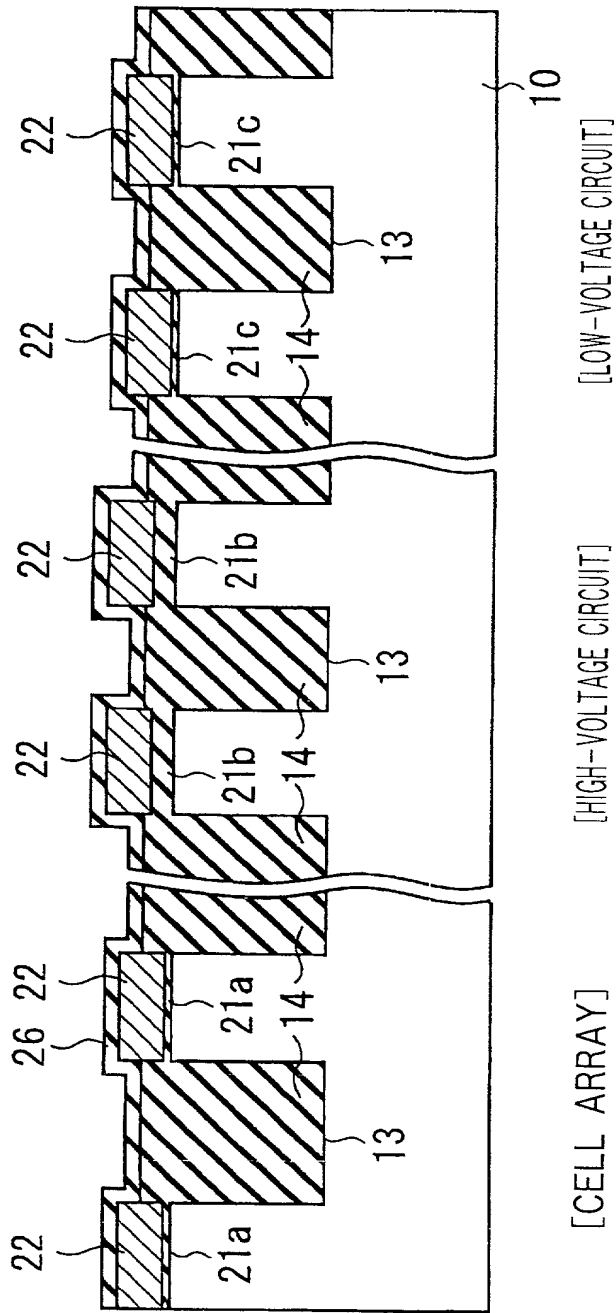


FIG. 26

FIG. 27

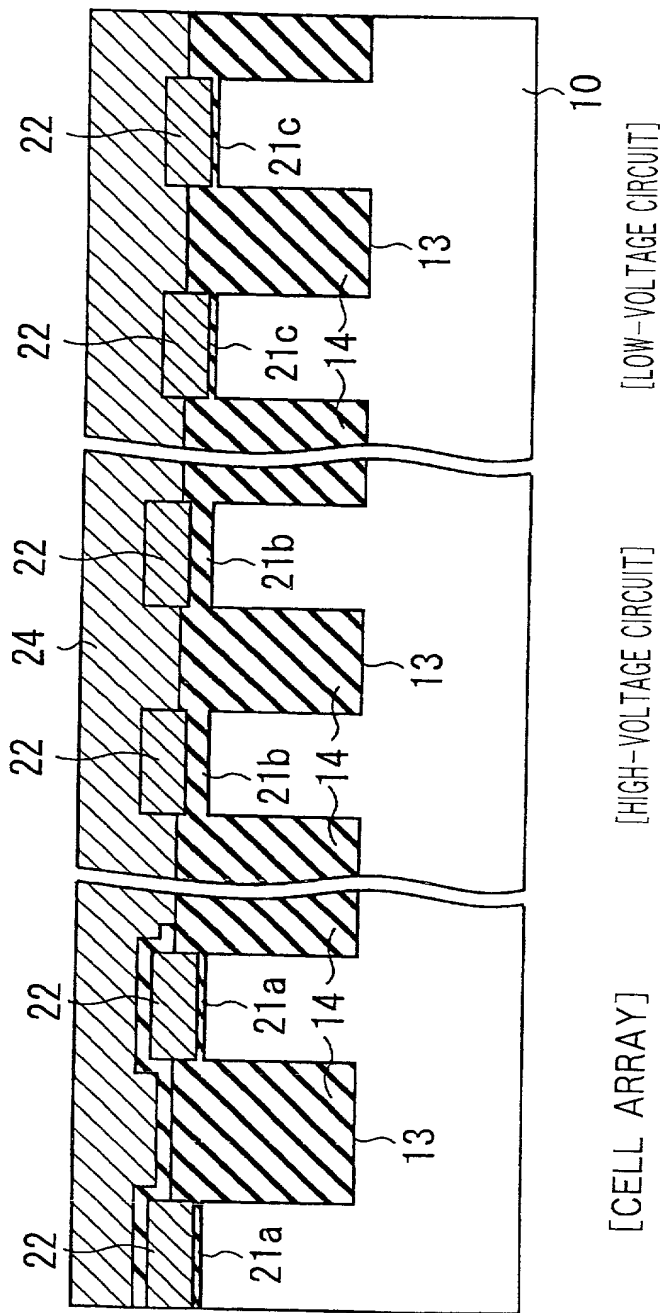


FIG. 28

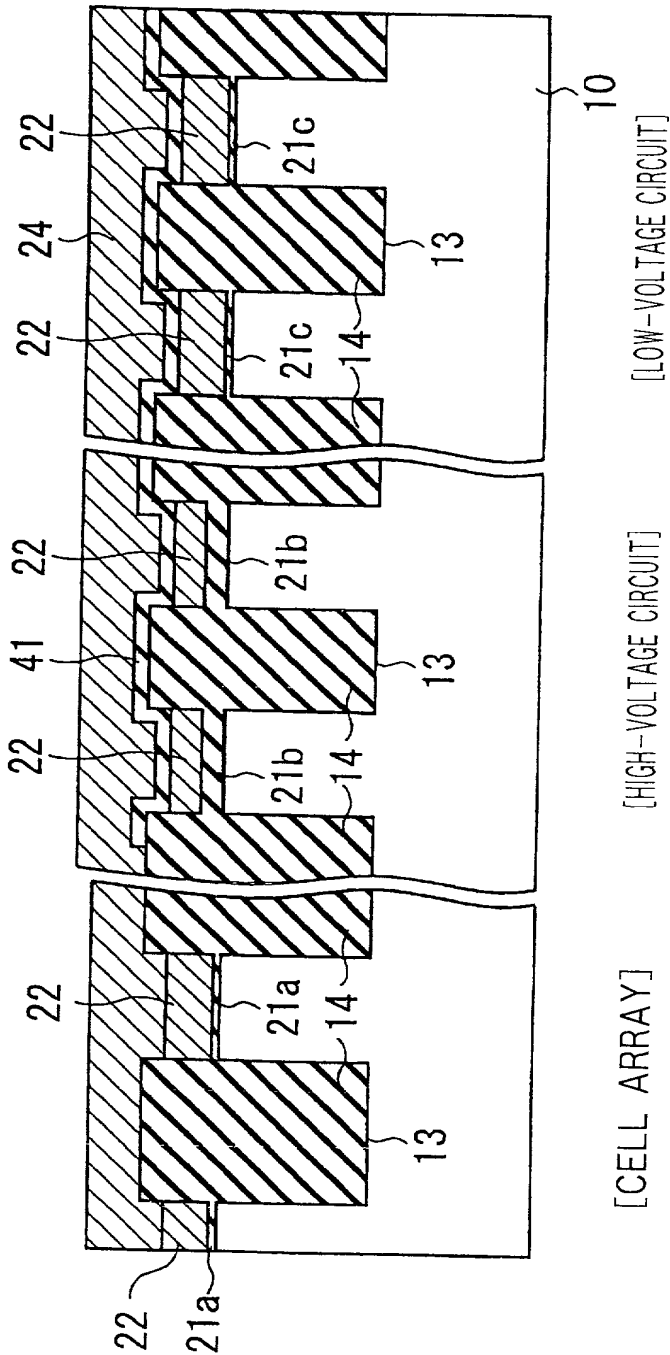


FIG. 29

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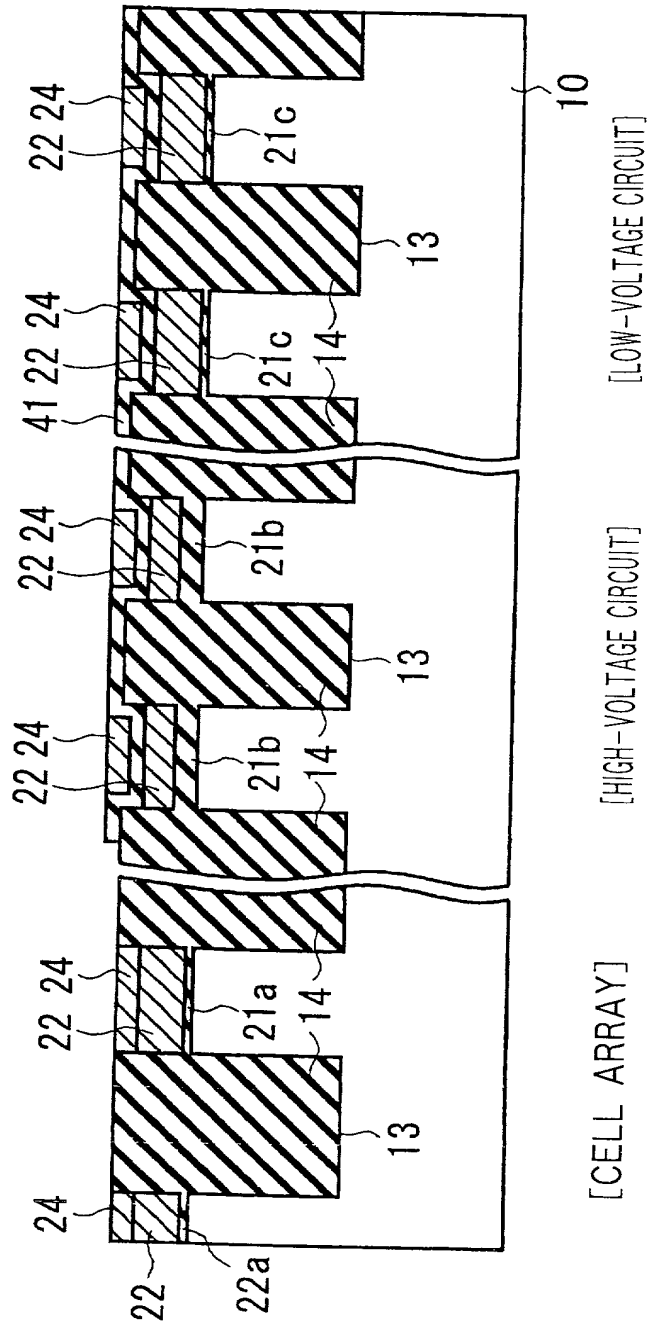


FIG. 30

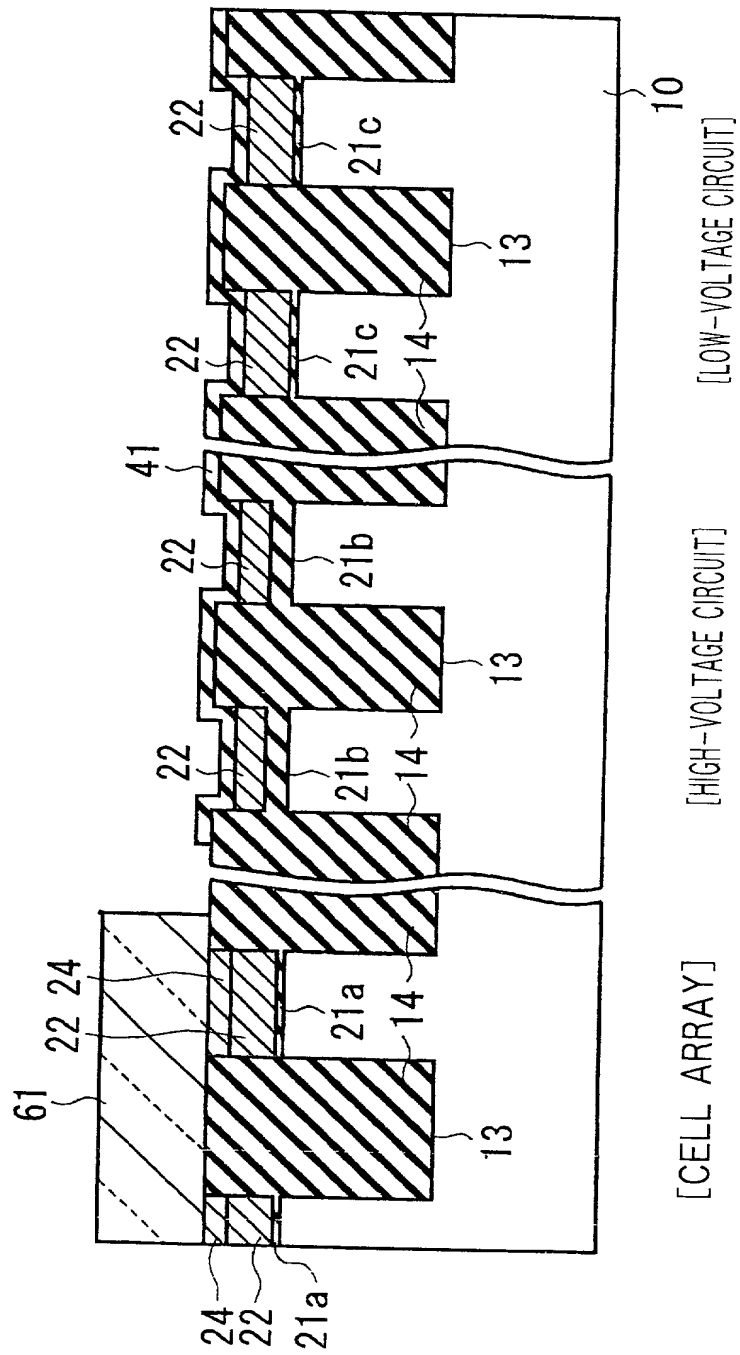


FIG. 31

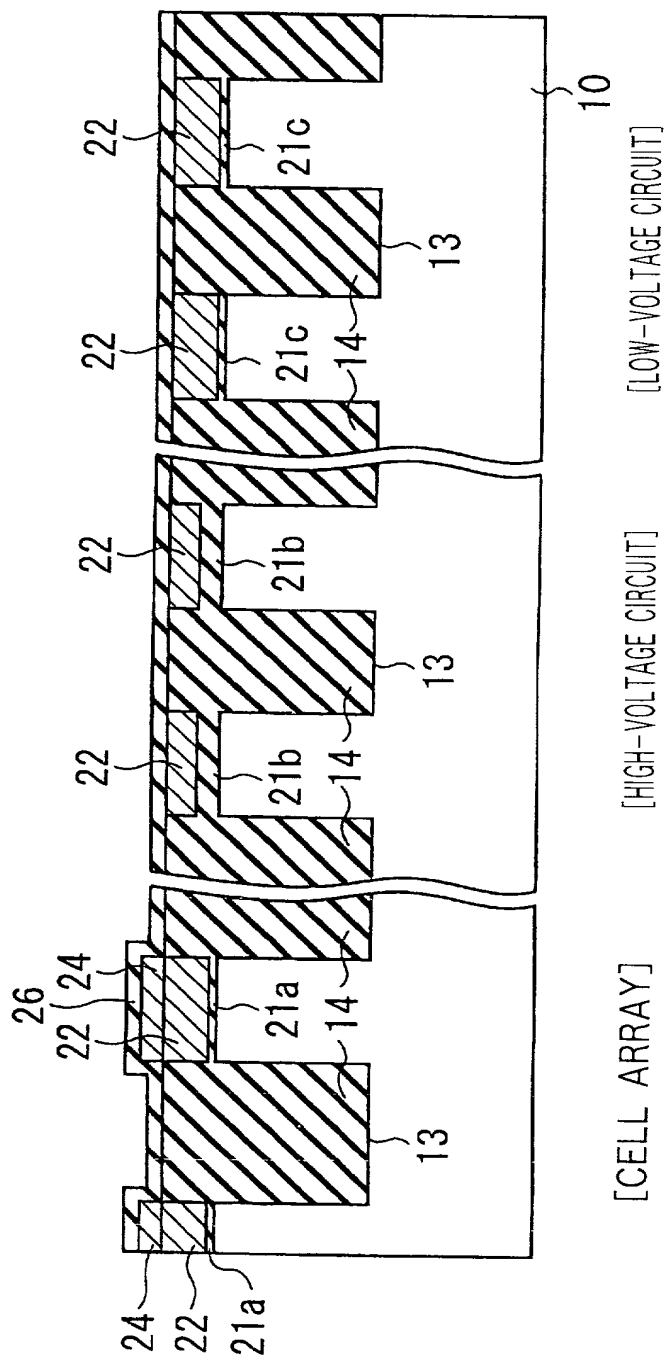


FIG. 32

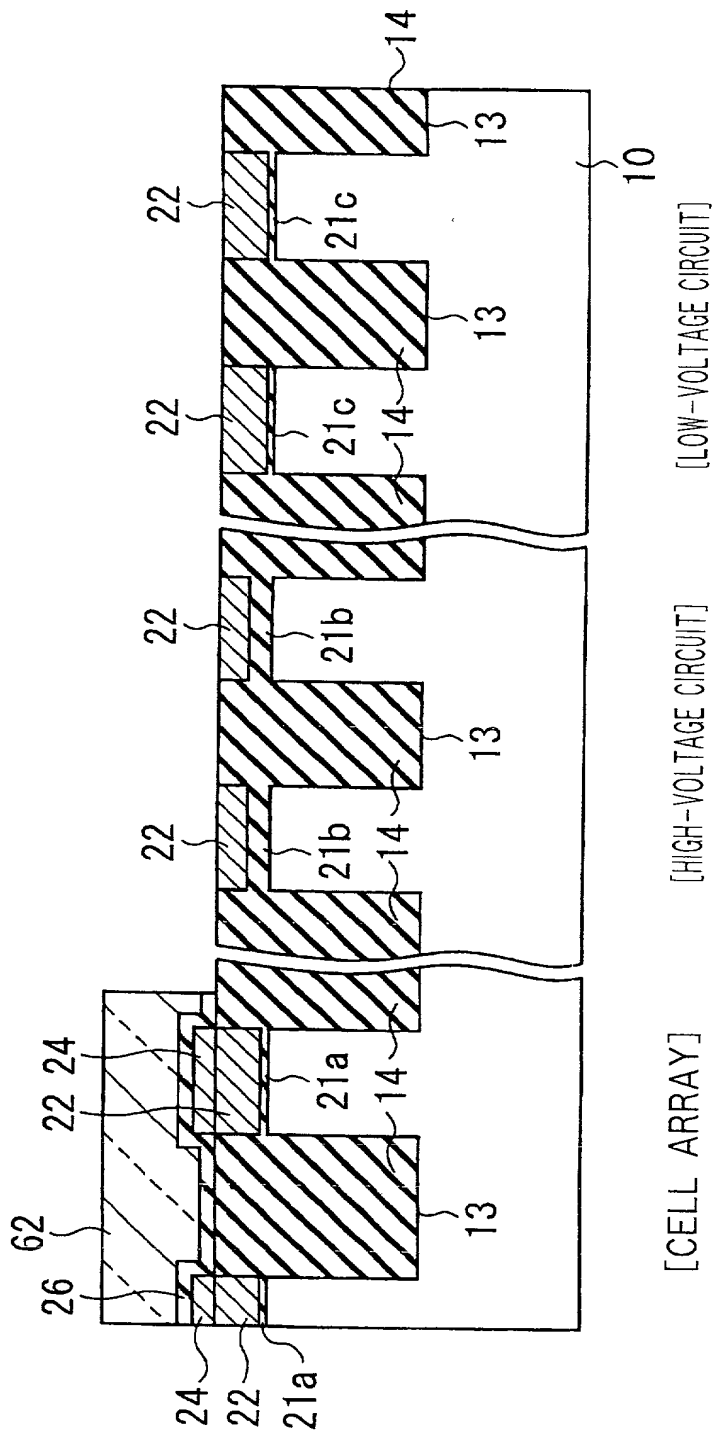


FIG. 33

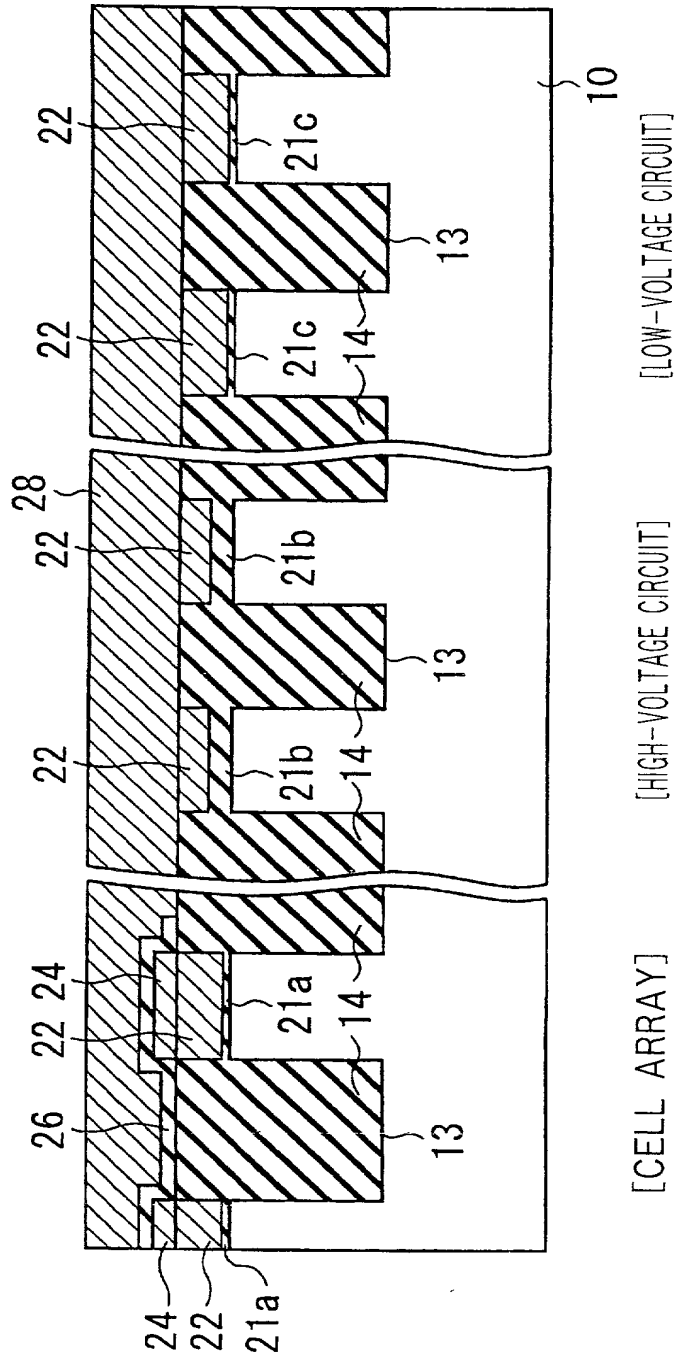


FIG. 34

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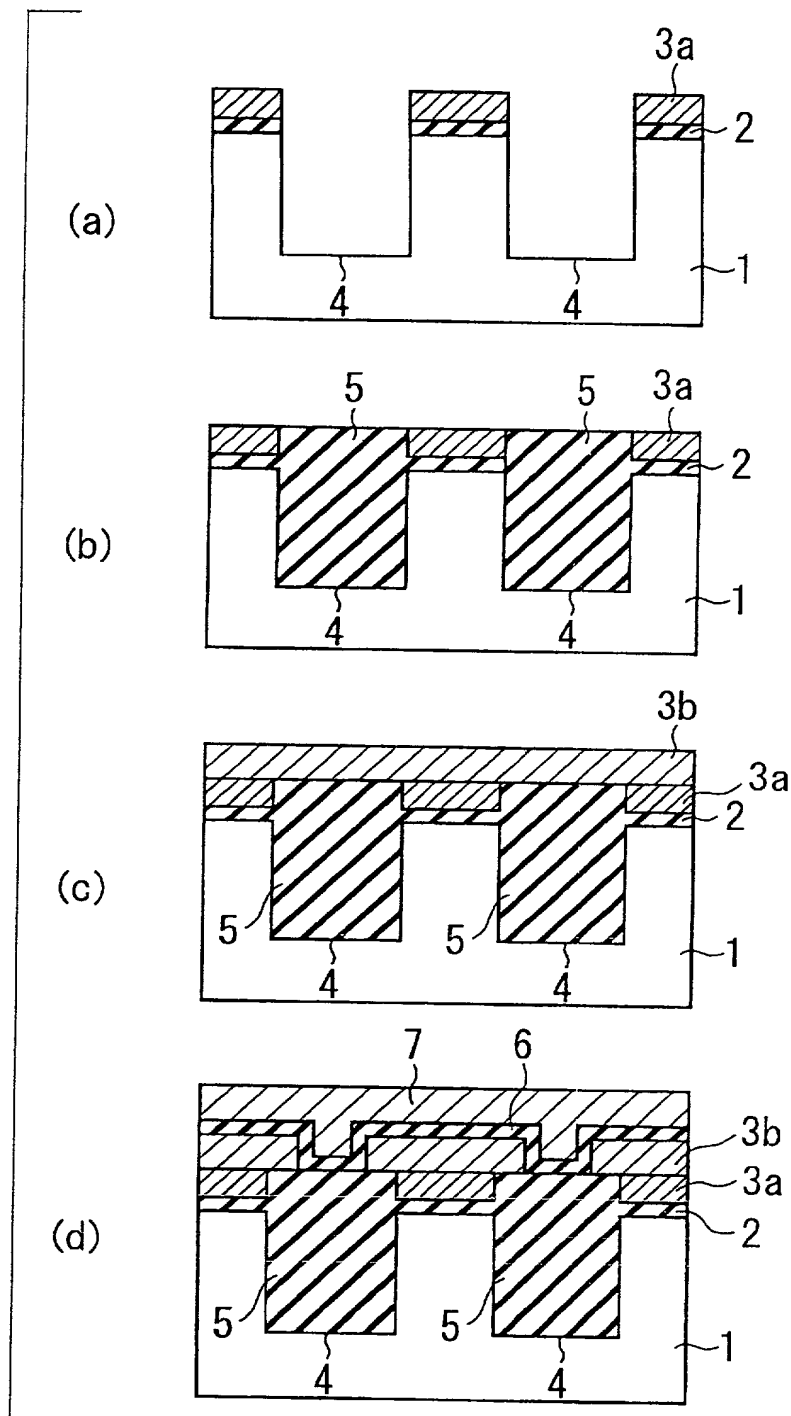


FIG. 35

FIG. 35

